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Asynchronous Design for Parallel Processing Architectures

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Goal: The objective of this research is to provide an interconnect design synthesis methodology which facilitates a modular design approach without compromising the global performance. The main tasks of this effort will be the development of the theory for optimal interconnect synthesis from a high-level specification, with emphasis on testability and fault-tolerance asynchronous interface among parallel computing hardware objects, and the application of this design methodology to physical implementations of multi-processing systems.

Progress:

1. Self-Timed Circuits Synthesis with Timing Constraints

   We started this project on incorporating timing constraints into the synthesis process of asynchronous interconnection circuits. The objectives are to optimize circuit delays and to reduce circuit hardware. The synthesis result shows that this strategy can yield significant improvements in circuit speed compared to the more conservative delay-insensitive design.

   The synthesis algorithm uses the CSP (Communicating Sequential Processes) language for circuit behavioral description, converts that description to a Petri net, and maps hardware delays onto the Petri net before performing circuit optimization. The algorithm proceeds the synthesis from a most conservative delay-insensitive and then relax the condition. This approach is different from that of using timing constraints for direct synthesis without verification of the circuit's correctness.

   By introducing timing information into the synthesis process, we eliminate redundant causal relations in a given specification by detecting the necessary and sufficient cause of a transition. Through Boolean algebra manipulations, a circuit of more concurrency can be synthesized. The resulting circuit is not hazard-free under all timing conditions, but if the given timing constraints are met, the circuit is guaranteed to work correctly.

   We have synthesized a few standard asynchronous interface circuits with a given set of timing constraints. The resulting circuits demonstrate an average of 30% decrease in execution time [1]. A self-timed VME bus interface was derived using this method, resulting in a much simpler design compared to a delay-insensitive one.

2. Inter-Chip Synchronization through Dynamic Delay Adjustment

   As an alternative to asynchronous handshake circuits for inter-chip interconnection, we have also studied the possibility of applying techniques of phase lock loops, as often used in telecommunications, to circuit interconnection. The strategy is characterized by a global clock frequency distribution coupled with a local on chip phase lock loop that provides a platform of dynamic delay adjustment for each input signal to be phase locked with the distributed global clock.

   The idea is not new, but has only been introduced to the VLSI society recently. The challenges are on the efficient design of the phase lock loop and on minimizing the effect of metastability in a phase detector that has to be included on each input pad. This scheme allows reliable high speed communication directly between ICs independent of the propagation delay between chips. The circuit design of an on-chip phase lock loop and an area-efficient implementation of a phase detector have been devised [2].

3. The Asynchronous Circuit Synthesis Program in C

We had previously programmed our synthesis algorithm in LISP. A C version of the synthesis program has recently been completed. Distribution of this program to AT&A, Berkeley, Univ. of Utah, and others for use in courses on asynchronous circuit design will be taped out in January 1990.

With the C version program, we can handle the synthesis of much bigger and more complicated circuits. The program provides an automated tool on which future research on asynchronous circuit design will be based on and tested against.

Future work in the next 2 quarters:

Since we have layouted an infrastructure for asynchronous interconnection circuit synthesis, the focus of research for the next two quarters will be toward theoretic pursuits. Even though we can be sure of the Boolean expressions synthesized from our algorithm being delay-insensitive, the translation of a Boolean expression to its gate level implementation is not a trivial task, for there could be multiple equivalent gate-level implementations for a particular Boolean expression. We would like to derive the necessary and sufficient conditions on the existence of a hazard-free gate level implementation given a Boolean expression. It is known that in general there does not exist a corresponding hazard-free implementation for "any" Boolean expression without changing the circuit's functionality. But given that we are only interested in a restricted set of all possible Boolean expressions, namely, those synthesizable by our algorithm, we would like to guarantee an implementation if possible. It is hoped that this question will be answered through studies in classic circuit hazards with the aid of graph theory and Boolean algebra.

We will also put emphasis on synthesis for testability as our next goal. Testability has become a major design consideration in IC industry and the question that whether asynchronous circuits will simplify the testing tasks is to be answered. Furthermore we will exploit the design domain from the synthesis point of view, so that we can construct testable asynchronous circuits with guaranteed coverage.

References

[1]. Teresa H.-Y. Meng and Dwight Joe, "Asynchronous Self-Timed Circuits Synthesis with Timing Constraints", IEEE ISCAS 90, May 1990.

[2]. Jim Goetz and Teresa H.-Y. Meng, "Inter-Chip Synchronization through Dynamic Delay Adjustment", IEEE ISCAS 90, May 1990.